AMENDMENTS TO THE SPECIFICATION

Please replace the paragraph beginning on line 13 of page 8 of the instant application with the following amended paragraph:

Figure 6 is a block diagram illustrating a preferred embodiment of a multi-processor system 60 including the cross bar multipath resource controller in accordance with the invention that includes a cross bar multipath memory controller 62 and a cross bar multipath peripheral controller 64. The details of the cross bar multipath memory controller 62 is described below with reference to Figures 7 and 8 and details of the cross bar peripheral controller 64 is described below with reference to Figures 9 and 10. As shown, the system 60 may include a host processor 66 which may preferably be a reduced instruction set (RISC) ARM core made by ARM Inc and a coprocessor core 68 that operate in a cooperative manner to complete tasks as described above. In the preferred embodiment, there may also be a hardware accelerator engine 70 as shown. The host processor, the coprocessor and the hardware accelerator engine are all connected to the multipath memory controller 62 and the multipath peripheral controller 64 as shown. To control access to the shared resources connected to the multipath memory controller and the multipath 25 peripheral controller, the system 60 may include a semaphore unit 72 which permits the two processors 66, 68 to communicate with each other and control the access to the shared resources. ~~The details of the semaphore unit is described in more detail in copending US patent application number XX/XXX,XXX filed on XXXX,XX 2001 titled "XXX" and incorporated herein by reference.~~ The semaphore unit permits the processors to negotiate for the access to the shared resources as described

above, but then, due to the multipath controllers 62, 64, permits the processors to access the resources over its own bus that is part of the controllers. To control the timing of the controllers 62, 64, a timer/clock 74 is connected to each controller 62, 64.